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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/604,301	06/26/2000	Yusuke Tsutsui	81784.0210	3587

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EXAMINER	
NGUYEN, HAU H	

ART UNIT	PAPER NUMBER
2676	9

DATE MAILED: 06/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/604,301	TSUTSUI ET AL.	
	Examiner	Art Unit	
	Hau H Nguyen	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4, 8-11, and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Kinoshita et al. (U.S. Patent No. 5,771,031).

Referring to claims 1, 8, 10, Kinoshita et al. teach a display panel having a plurality of pixels arrayed in a matrix, the pixels in each row forming one horizontal pixel array; a plurality of block driving circuits arranged in series to divide pixels in each horizontal pixel array to a plurality of pixel blocks, for driving the pixel blocks, respectively (col. 2, lines 11-17). As shown in Fig. 3, Kinoshita et al. teach each of the driver sections XT1 to XT8 is constituted by a shift register circuit SR of 100 stages (or bits) (input-side line memory), a selection circuit SA, a latch circuit LA1, a latch circuit LA2 (output-side line memory), and a digital-analog converter D/A (col. 6, lines 39-42). Assignment of input data into display regions is depicted in Fig. 5. Kinoshita et al. also teach in the driver section XT1, first to hundredth stages of the shift register store a start pulse ST in turns in response to clock pulses CK. The selection circuit SA selects corresponding one of hundred RGB pixel data items sequentially supplied to data supply bus SDL1 as a RGB pixel-data block DB1, in response to a signal from a stage which stores the start pulse ST, and supplies three pixel data items of the selected RGB pixel data to the latch circuit

LA1, simultaneously. The latch circuit LA1 latches each of pixel data items sequentially supplied from the selection circuit SA in correspondence with hundred RGB pixel data items, and supplies the pixel data items into the latch circuit LA2. The latch circuit LA2 latches all the pixel data items from the latch circuit LA1 in response to a load pulse LD, and supplies the pixel data items to the digital-analog converter D/A. The digital-analog converter D/A converts the pixel data items into pixel signal voltages, respectively, and supplies to signal lines X1 to X300 (col. 10, lines 51-67, and col. 11, lines 1-2).

In regard to claim 2, as cited above, Kinoshita et al. teach the pixels in each row forming one horizontal pixel array; a plurality of block driving circuits arranged in series to divide pixels in each horizontal pixel array to a plurality of pixel blocks, for driving the pixel blocks. Thus, the number of the memory portions is determined corresponding to the number of regions divided in a horizontal direction.

In regard to claims 3-4, and 11, with reference to Fig. 3, Kinoshita et al. teach each shift register circuit SR sequentially shifts a start pulse ST to the next stage, in response to a clock pulse CK. Each selection circuit SA extracts RGB pixel data SD of 18 bits from the data supply bus SDL2 in response to a start pulse from each stage of a corresponding shift register circuit SR, and supplies R, G, and B pixel data items of six bits contained in the extracted RGB pixel data SD in parallel to a corresponding latch circuit LA1. Each latch circuit LA2 (output-side shift register) latches pixel data items for 300 pixels from the latch circuit LA1 in response to a load pulse LD, and supplies the pixel data items for 300 pixels to a corresponding digital/analog converter D/A. Each digital-analog converter D/A converts pixel data items for 300 pixels into

pixel signal voltages and supplies the pixel signal voltages to 300 corresponding signal lines (col. 7, lines 8-21).

Referring to claims 9 and 19, as shown in Fig. 5, data is supplied every horizontal scanning period, and parallel data transfer is performed during a horizontal blanking period.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinoshita et al. (U.S. Patent No. 5,771,031).

Referring to claims 5-7, as applied to claim 1 above, Kinoshita et al. teach all the limitations of claims 5-7, except for the data storage capacities of the input and output line memory correspond to 400 pixels or 512 pixels, and starting the data items from the 400^{th}, 320^{th}, and 256^{th}. However, it would have been an obvious matter of design choice to modify the size of the line memory and the order of the output-side memory as taught by Kinoshita et al. corresponding to 400 pixels or 512 pixels, starting the data items from the 400^{th}, 320^{th}, and 256^{th} since applicant has not disclosed that having the size of line memory corresponding to 400 or 512 pixels, or starting the data items from the 400^{th}, 320^{th}, and 256^{th} solves any stated problem or is for any particular purpose because the size of line memory will vary based on the amount of

data being processed or displayed, and the driver sections XT1 to XT8 is performed independently, and it appears that any memory size and any order of input data items would perform equally well.

5. Claims 12-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinoshita et al. (U.S. Patent No. 5,771,031) in view of Asada (U.S. Patent No. 6,020,871).

Referring to claims 12-14, 16, as cited above, Kinoshita et al. teach all the limitations of claims 12-14, except that the output-side line memory further includes a shift direction for switching the data output in forward or reverse direction.

However, Asada teaches a bi-directional scanning circuit applicable when a plurality of IC chips are connected in cascade. As shown in Figs. 1 and 10, the direction of the scanning circuits can be performed leftward or rightward.

Therefore, it would have been obvious to one skilled in the art to utilize the driving circuits as taught by Asada in combination with the driving circuit as taught by Kinoshita et al. in order to achieve a high speed bi-directional scanning circuit (col. 3, lines 16-18).

In regard to claim 15, since the display unit as taught by Kinoshita et al. is a flat panel display, data items can be digital video signals.

Referring to claims 17-18, as applied to claim 13 above, Kinoshita et al. and Asada teach all the limitations of claims 17-18, except that the numbers n and k are any of 512, 400, 320, and 256, and the number of memory portions is equal to the product of the number of regions divided in a horizontal direction and the number of primary colors. However, it would have been an obvious matter of design choice to modify the size of the line memory and the number memory portions as taught by Kinoshita et al. and Asada corresponding to 512, 400, 320, and 256, and the

number of memory portions as claimed since applicant has not disclosed that having the size of line memory and the number of memory portions solves any stated problem or is for any particular purpose because the size of line memory will vary based on the amount of data being processed or displayed, and the driver sections XT1 to XT8 is performed independently, and it appears that any memory size and memory portions would perform equally well.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

H. Nguyen

06/12/2003

Matthew C. Bella

MATTHEW C. BELLA
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